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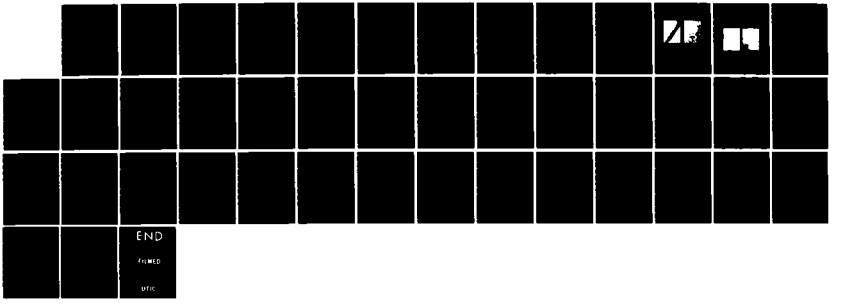

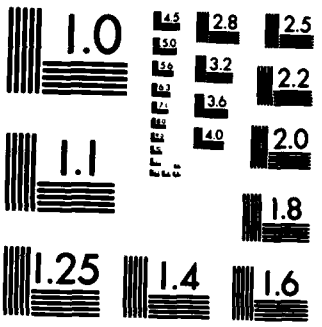

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MATERIALS–PROCESS INTERACTIONS IN TERNARY ALLOY SEMICONDUCTORS

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Properties of InGaAs, implantation doping of InGaAs, Photoluminescence Properties of InGaAs, surface studies on InGaAs, X-ray photoelectron spectroscopy and electron energy loss spectroscopy studies on InGaAs. The report describes the electrical and optical properties of $In_{0.53}Ga_{0.47}As$ layers grown by liquid phase epitaxy on InP substrates. The report also describes ion implantation doping experiments to form n- and p-type layers in $In_{0.53}Ga_{0.47}As$. High degree of n-type electrical activation can be achieved in Si-implanted samples. Formation of p-type layers by Be- or Mg-ion implantation is much more difficult.

X-ray photoemission (XPS) and electron energy loss (ELS) studies show that the native oxides present on chemically etched $In_{0.53}Ga_{0.47}As$ consist predominantly of As_2O_3 and oxides of In. Plasma enhanced deposition of SiO_2 at 300°C does not significantly →

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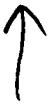
change the thickness of the native oxide. Although capacitance-voltage measurements on the MIS capacitors on $In_{0.53}Ga_{0.47}As$ exhibit high, the surface potential can be modulated. PECVD SiO_2 appears to be a viable candidate as a gate dielectric for $In_{0.53}Ga_{0.47}As$ MISFETs.



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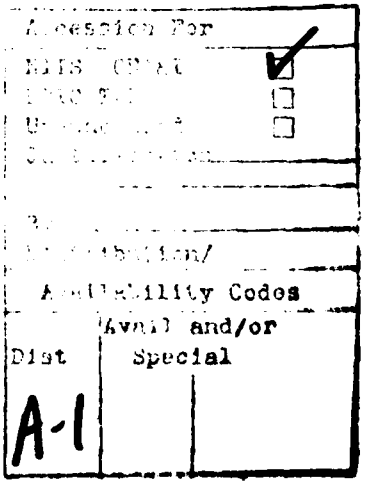

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SECTION 1

INTRODUCTION

Recent improvements in optical fiber technology have resulted in the availability of fibers exhibiting low loss and low dispersion in the 1.2 to 1.6-μm range. These fibers are also radiation resistant and are expected to play a major role in long baseline, high speed, secure communication systems. The availability of reliable semiconductor light sources and detectors capable of operating in this wavelength range is crucial to the development of such systems.

Experimental results suggest that photodiodes fabricated in $In_{0.53}Ga_{0.47}As$ (lattice-matched to InP substrates) can be efficient detectors for this desired wavelength range. For such systems applications, it is desirable to integrate the detectors with circuits capable of performing signal processing functions. These circuits can either be fabricated in InGaAs epitaxial layers or in InP substrates. To accomplish such a level of integration, a mature process technology in InGaAs must be developed. The device technology in this alloy system is in a truly primitive state. The primary objective of this program is to develop a reliable and mature process technology in InGaAs. Particular attention has been to ion implantation doping of InGaAs and the study of dielectric-sesmiconductor interfacing so that InGaAs MISFET device and photodetector technology can be established.

SECTION 2

EPITAXIAL GROWTH AND CHARACTERIZATION OF InGaAs

A. INFINITE SOLUTION EPITAXIAL GROWTH

As discussed in our earlier progress reports, the infinite solution epitaxial growth technique developed at Hughes Research Laboratories (HRL) is capable of growing large number of epilayers with reproducible electrical and optical properties from the same solution. We have used this technique to grow layers of GaAs, (Aℓ,Ga)As, InP and (Hg,Cd)Te from an approximate matrix. In this section we discuss the experiments performed to apply this technique in the growth of lattice-matched $In_{0.53}Ga_{0.47}As$ layers on InP substrates.

The epitaxial growth system is illustrated schematically in Figure 1. It consists of the quartz growth tube connected by a high-vacuum valve to a stainless-steel entry chamber. A saturated solution of the appropriate elements is contained in a crucible and serves as the growth matrix. Once a specific solution has been prepared, it is kept in a paladium-purified hydrogen ambient. It can be maintained at or near the growth temperature in a controlled environment for long periods of time. During this period, a long series of runs with all operations such as adding dopants or introducing substrates for epigrowth are performed by passing these materials through an entry chamber. This chamber can be independently evacuated and flushed with hydrogen before opening to the growth tube. Thus it is possible to change one variable at a time and keep all the other variables under control. We have used this system to grow high purity InP layers in the presence of controlled amounts of water vapor in growth ambient.

The heteroepitaxial growth of lattice-matched $In_{0.53}Ga_{0.47}As$ on InP is a difficult problem. The growth temperature has to be low enough to ensure that there is little or no interdiffusion of the constituents of the InGaAs epilayer and the InP substrate.

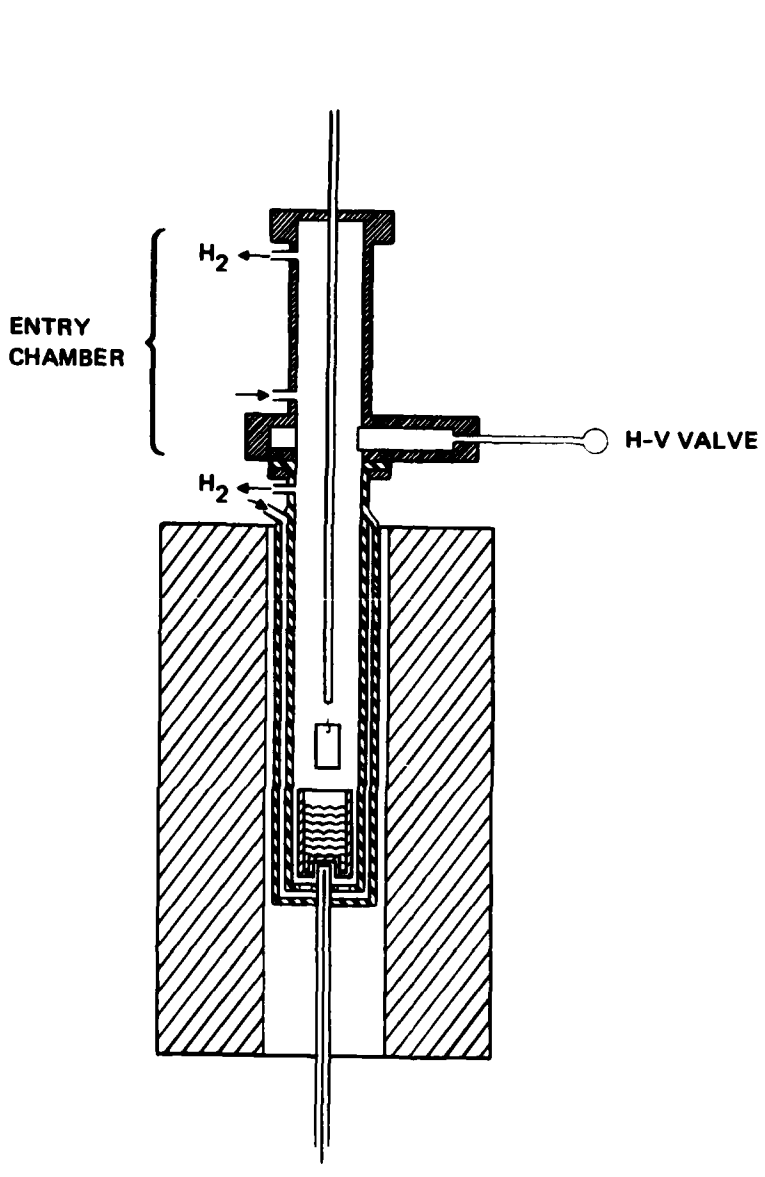

Figure 1. Schematic of LPE growth system.

The presence of such undesired interdiffusion will result in the formation of variable composition InGaAsP quaternary alloys. Loss of phosphorus at high growth temperatures will degrade the quality of the InP substrates prior to growth . This can lead to the presence of a conducting In-rich layer at the heterointerface. This in turn, will severely degrade the quality of InGaAs epitaxial layers. By modifying our infinite solution growth system, we have ensured that the surface degradation of InP is minimized. The results are discussed below.

During the growth of InP epitaxial layers, we observed severe degradation of InP substrates. Prior to growth, it is essential to maintain the substrate holder (with the substrate) in the hydrogen ambient above the solution in order to ensure that thermal equilibrium is maintained with the solution. This prewarming step is necessary to prevent sponta-neous nucleation around the substrate holder upon immersion into the solution. During this prewarming step we observed severe surface degradation of InP substrates, primarily as a result of loss of phosphorus. Such surface degradation can adversely affect the heterointerface in the growth of InGaAs on InP. To avoid such interface problems, we have modified our sample holder, permitting us to maintain an ambient of dilute phosphine over the sample. The ability to maintain such a controlled ambient over the sample during the warming cycle will prevent any loss of phosphorus and thus reduce surface degradation.

Micrographs illustrating such surface degradation are shown in Figures 2(a) and (b). The InP sample was held above the solution in flowing hydrogen ambient at 730°C for 90 min. Thermal etch pits can be clearly seen. The pitted regions are In rich and occur as a result of loss of phosphorus during the high temperature process step (Figure 2(b)). For comparison we have shown the surface features of the substrate (Figure 2(a)) prior to heat treatment. Figures 3(a) and (b) show the surface morphology of a sample subjected to the same heat treatment with the

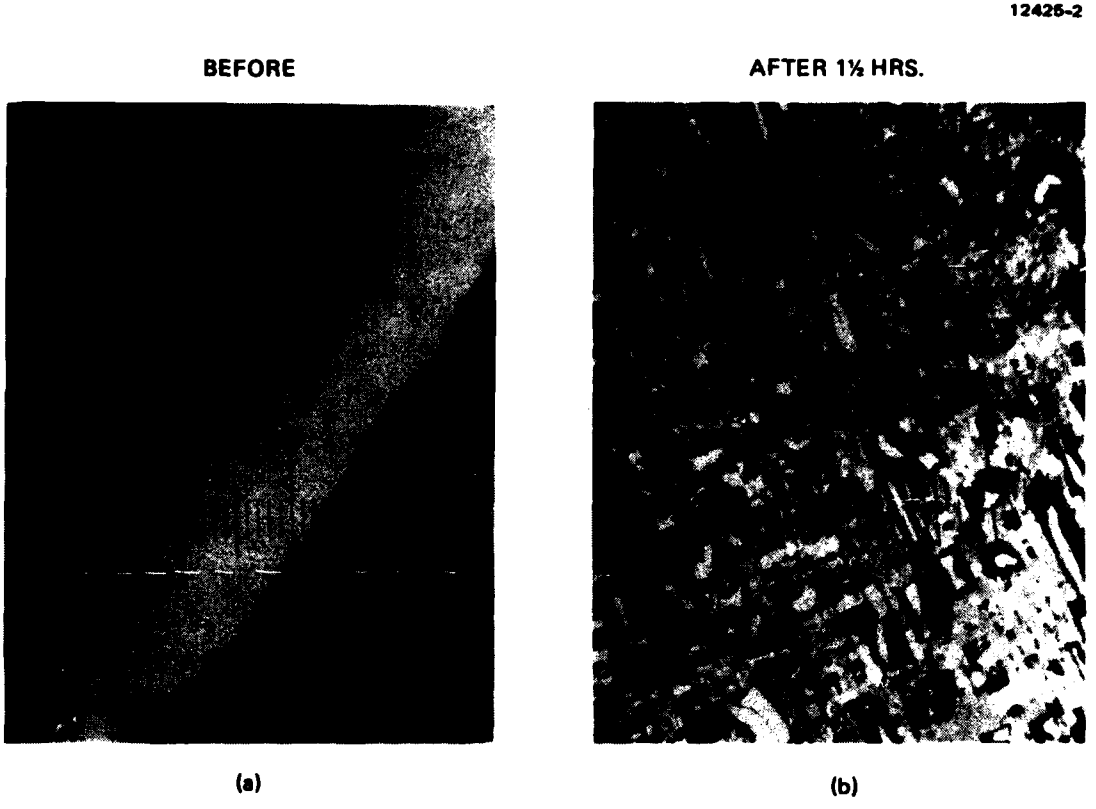

Figure 2. Decomposition of InP substrate at 730°C in H_2 ambient.

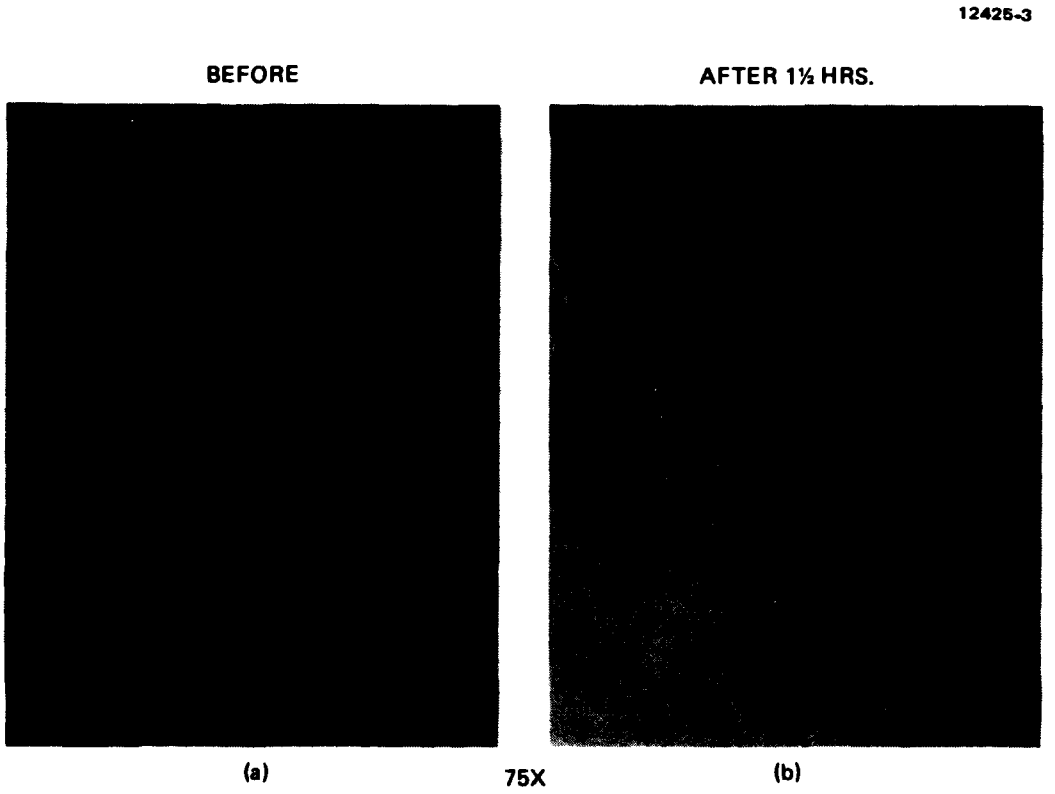

Figure 3. Decomposition of InP substrate at 730°C in H_2 ambient with PH_3.

sample maintained in flowing phosphine ambient. Figure 3(a) shows the surface morphology of the sample prior to heat treatment, while Figure 3(b) shows the surface morphology after heat treatment. This micrograph clearly demonstrates that maintaining InP substrates in an ambient of flowing phosphine prior to epigrowth can suppress surface degradation.

To ensure that there are no major problems associated with leaks in the system, we grew high purity GaAs layers in the modified system. We then attempted to grow InGaAs layers on GaAs substrates using a solution with an In:Ga ratio of 4:1. Severe problems arose because InP oxidizes more readily than GaAs. Also indium oxides cannot be reduced in hydrogen below ~600°C. Extensive precautions were taken to minimize the oxygen contamination in the system and the experiments were repeated at a growth temperature of 650°C. Extensive baking of the solution was carried out. As a result of these procedures we were able to grow layers with carrier concentrations in the mid-10^{15} cm^{-3} range with an In content of ~0.05%.

After the preliminary studies, a new solution was prepared with a Ga composition of 0.0251 mole fraction in solution. The growth temperature was chosen to be ~650°C. After adding the solute the solution was heated and cycled up and down in temperature to ensure complete mixing. The total weight of the solution was ~800 gm. The InP substrate was introduced slowly into the solution and the substrate and the solution were thermally equilibrated prior to initiating the growth. For the growth conditions employed, the growth rate was rather rapid (~1 μm/min). Layers of ~4 μm thick were grown. Electron microprobe measurements on these layers indicated that the composition was ~$In_{0.56}Ga_{0.44}As$. The layers were n-type with room temperature electron concentrations of ~1 x 10^{-7} cm^{-3} and electron mobilities of ~6900 cm^2 V^{-1} s^{-1}. Several repeated attempts to improve the surface morphology, composition and electrical properties of the epitaxial layers clearly showed that considerable experimental effort is required to apply infinite solution

epitaxy to grow $In_{0.53}Ga_{0.47}As$ layers. Consequently, to carry out the experiments stated in this program, it was decided to purchase liquid phase epitaxial layers grown at Research Triangle Institute, Raleigh, NC. The layers were grown by a conventional horizontal slide bar epi-process. In the next section we describe the representative electrical and optical properties of these epitaxial layers.

B. EVALUATION OF InGaAs EPITAXIAL LAYERS

1. Introduction

InGaAs epitaxial layers can be lattice-matched to InP substrates at a composition of $In_{0.53}Ga_{0.47}As$. At alloy compositions far removed from the lattice-matched composition, severe lattice mismatch between the epi-layer and the substrate can occur. This will result in the generation of misfit dislocations and other crystallographic defects. These defects can affect the structural electrical and optical properties of the epitaxial layers.

2. Electrical Evaluation of InGaAs

The electrical properties of the InGaAs epitaxial layers grown at the Research Triangle Institute were evaluated by Hall effect measurements. The Hall samples were prepared by cleaving square-shaped samples and forming ohmic contacts at the corners by evaporating Au:Ge/Ni and then alloying them at 350° for 1 minute in a flowing forming gas ambient. This ensured that the contacts remained ohmic at low temperatures. The samples were all n-type and fell into two categories exhibiting a room temperature carrier concentration of ~5.1 x 10^{15} cm^{-3} and 2.4 x 10^{15} cm^{-3} with electron mobilities of ~9560 cm^2 V^{-1} s^{-1} and 10,780 cm^2 V^{-1} s^{-1}, respectively.

Hall effect measurements were also performed as a function of temperature using the HRL designed variable temperature Hall effect system. The electron concentration as a function of 1000/T is shown in Figure. 4. The data clearly show that the dominant donor energy level is quite shallow and that transport at low temperatures is dominated by impurity band conduction. This makes it difficult to estimate the degree of compensation in the material. The variation of electron mobility with temperature is illustrated in Figure 2. As the measurement temperature is lowered, the electron mobility increases from the room temperature value of 9560 $cm^2\ V^{-1}\ s^{-1}$ and reaches a maximum value of 27,000 $cm^2\ V^{-1}\ s^{-1}$ at ~60°K. At lower temperatures the mobility decreases. In the low temperature region, impurity scattering decreases the mobility, while lattice scattering is the dominant mechanism controlling the mobility in the high region. These electrical properties indicate that the layers are of device quality. The temperature dependence of the electrical properties from the second group of samples (carrier concentration of $2.4 \times 10^{15}\ cm^{-3}$, mobility of 10,780 $cm^{-2}\ V^{-1}\ s^{-1}$ at 300°K) were similar to those shown in Figures 4 and 5.

3. Photoluminescence Properties of InGaAs

The optical properties of the InGaAs epitaxial layers were evaluated by obtaining the photoluminescence spectrum from such a layer at 6°K.

The sample to be analyzed was mounted on the tailpiece of a Janis 11-DT varitemp dewar. The sample was illuminated with 641 nm of radiation from a coherent CR2000K Kr ion laser. The luminescence from the sample was focused onto the slits of a Spex 1404 double grating spectrophotometer. A Ge detector was used.

Figure 6 shows a typical PL spectrum from an $In_{0.53}Ga_{0.47}As$ sample. The emission band at ~0.87 eV is the near bandedge emission and is not clearly resolved.

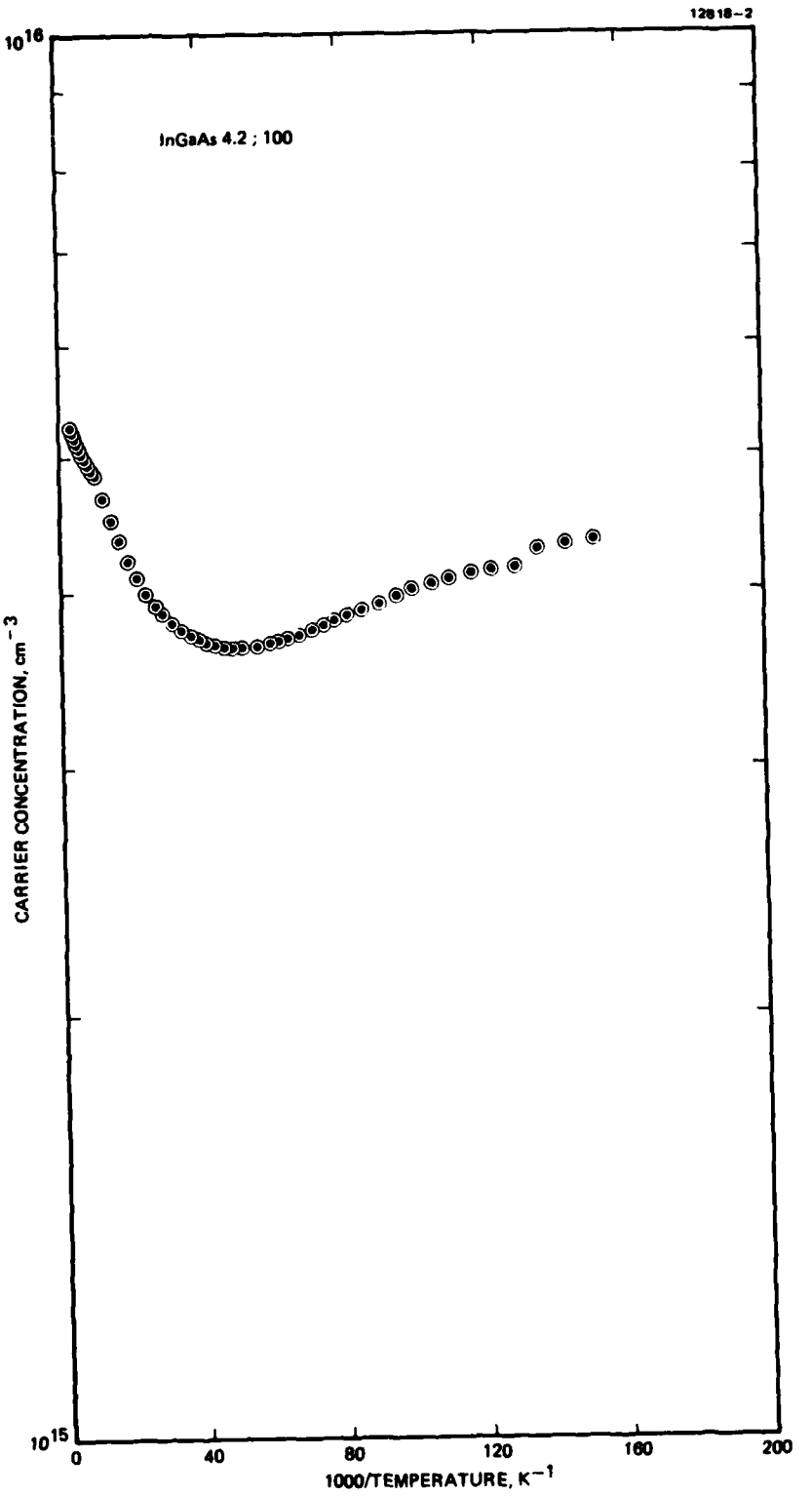

Figure 4. Carrier concentration as a function of inverse temperature (1000/T, K^{-1}) from an n-type $In_{0.53}Ga_{0.47}As$ sample.

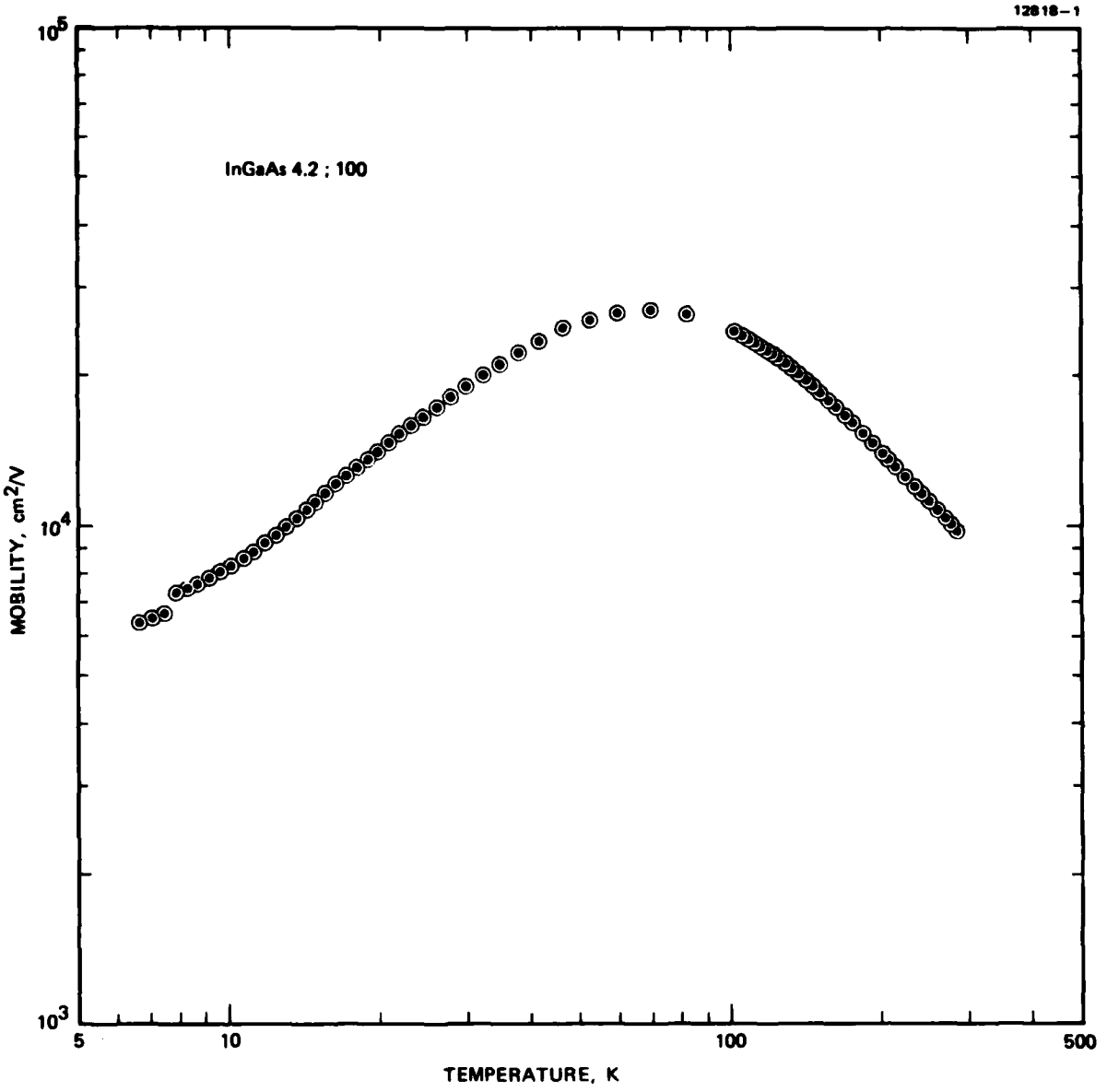

Figure 5. Variation of electron mobility with temperature from an n-type $In_{0.53}Ga_{0.47}As$ sample.

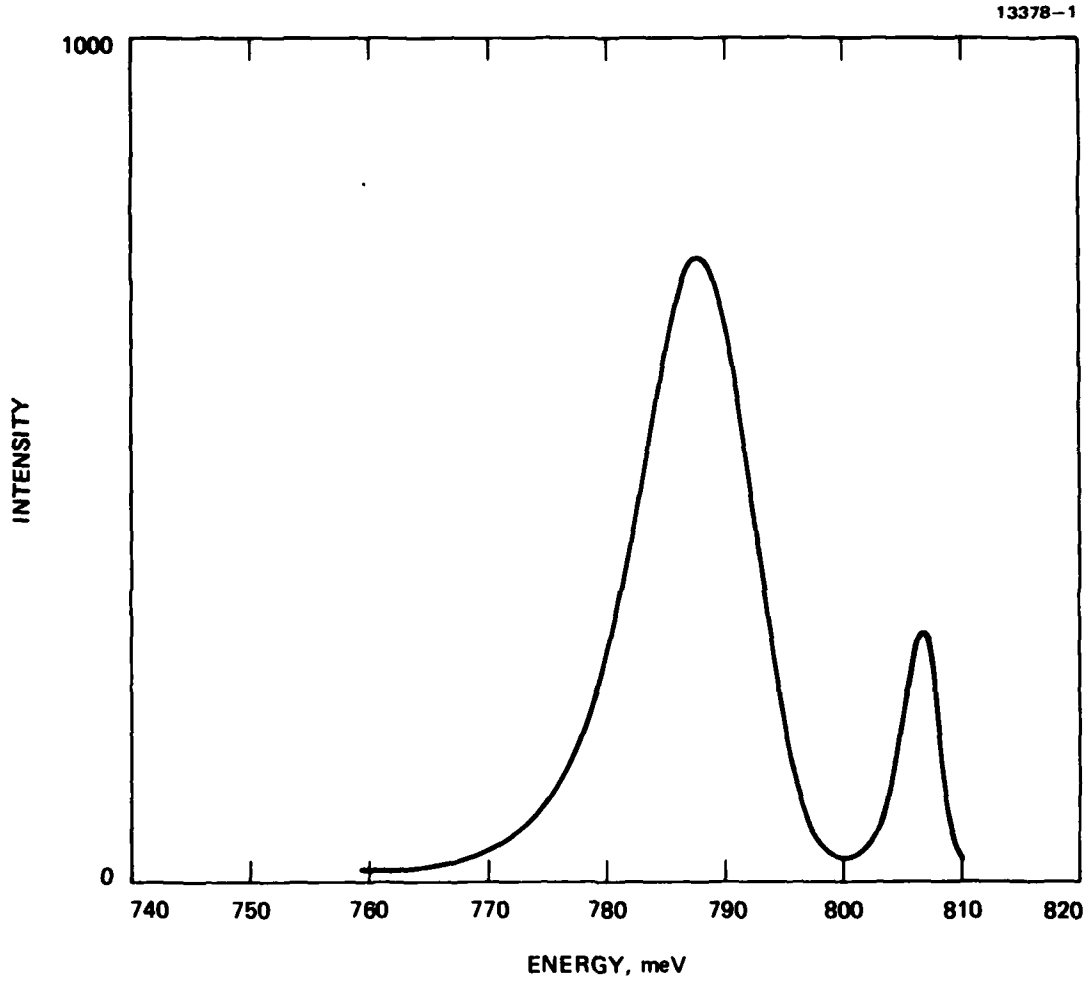

Figure 6. Photoluminescence (6K) spectrum from an $In_{0.53}Ga_{0.47}As$ sample.

We speculate that the lower energy band at ~0.786 eV is associated with donor-to-acceptor transitions. The wide unresolved peaks in this spectrum are characteristic of InGaAs epitaxial layers and agree reasonably well with some recently published data.[1] In the absence of any sharply defined features, it is difficult to assess the quality of the material using photoluminescence.

The eptiaxial layers exhibited electrical properties which were sufficiently high quality for use in implantation studies described in Section 3 and surface analysis studies described in Section 4.

SECTION 3

ION IMPLANTATION DOPING OF InGaAs

A. INTRODUCTION

The primary goals of this program are to identify the dopants which can be used to form p- and n-type layers in InGaAs by ion implantation and to identify the implantation and the annealing conditions required to electrically activate such doplants. Consequently, we chose to investigate the behavior of Be and Si as p- and n-type dopants in $In_{0.53}Ga_{0.47}As$.

B. P-TYPE IMPLANTS

Be is known to be the lightest mass p-type dopant in III-V semiconductors. Previous studies performed at HRL and other laboratories have shown that implanted Be can be activated following annealing at rather low tempera-tures (~480°C for GaAs and 550°C for InP.) Since lower processing temperatures result in improved control over the dopant profiles, we decided to investigate the annealing behavior of Be-implanted $In_{0.53}Ga_{0.47}As$ layers. Beryllium was implanted at an energy of 100 keV to a fluence of 1×10^{14} cm^{-2} into an 8.3-μm-thick n-type $In_{0.53}Ga_{0.47}As$ epitaxial layer ($n \simeq 2.4 \times 10^{15}$ cm^{-3}; $\mu e = 10,780$ cm^2 V^{-1} s^{-1} at room temperature prior to implantation) grown on semi-insulating InP. Following the implant, the wafer was cleaved to form several Hall samples measuring 3mm x 3mm. The samples were then encapsulated with ~100 nm of SiO_2deposited by a plasma enhanced chemical vapor deposition (PECVD) process. The samples were annealed for periods of 30 minutes at temperatures ranging from 550°C to 700°C in an ambient of forming gas. Following the anneal, the dielectric layer was removed and ohmic contacts to the sample were formed by using an In:Ag:Ge solder. The results of Hall effect measurements are summarized in Table 1. As seen from the table, no p-type activity was observed in samples annealed at 500°C, 550°C and 650°C. On annealing at 700°C, almost complete

Table 1. Electrical Properties of Be-Implanted InGaAs

T_A	Sheet Carrier Concentration	Carrier Mobility
550°C	- n-type	-
650	- n-type	-
700	(9.6 ± 0.04) x 10^{13} cm^{-2} p-type	87 ± 2 cm^2 V^{-1} s^{-1}

p-type activation was observed. This observed p-type doping behavior is not reproducible in all cases and appears to depend very strongly on the nature of the starting epitaxial layer. The observed experimental results may be strongly influenced by a leaky p-n junction interface. In such a case, the thick high conductivity n-type layers will dominate the measurements.

We also investigated the annealing behavior of Mg (another known p-type dopant) implanted in InGaAs. The results obtained were qualitatively similar to Be-implanted InGaAs. In samples which exhibited p-type conductivity, almost complete activation was observed for 1 x 10^{14} cm^{-2} implants after annealing at 750°C. This highly non-reproducible electrical activation of p-type dopants in InGaAs introduced by ion implantation has been observed by other workers. Recently, Gill and co-workers[2] studied the nature of residual defects present in ion-implanted InGaAs samples. They observed a very dense cluster of dislocation loops in samples which could not be doped p-types. Such dense loops were not present in samples which exhibited p-type doping behavior. The origin of these defects is not clear. Nevertheless, activation of p-type dopants in InGaAs is an extremely difficult problem and more work needs to be performed to develop a detailed understanding.

C. N-TYPE DOPING

Silicon is known to be an efficient donor in both GaAs and InP. We therefore decided to investigate the behavior of Si-ion

implanted $In_{0.53}Ga_{0.47}As$. Si ions of 100 keV were implanted to fluences ranging from 5 x 10^{12} cm^{-2} to 1 x 10^{14} cm^{-2}. After the implant, the samples were encapsulated with 100 nm of SiO_2 and were annealed at 700°C for 30 min in an ambient or flowing forming gas. Hall effect measurements were made on these samples after removing the dielectric and forming appropriate ohmic contacts. The data show that a high degree of electrical activation with higher electron mobilities can be achieved in the Si-implanted layers. The variation of measured electron concentration is shown as a function of implant fluence in Figure 7. As can be seen for the doses covered in this study, a high degree of electrical activation can be achieved. The measured electron mobilities range from ~8730 cm^2 V^{-1} s^{-1} for low fluence implants to ~4500 cm^2 - V^{-1} s^{-1} for high dose implants. We also investigated the rapid thermal annealing behavior of Si-implanted $In_{0.53}Ga_{0.47}As$. In a conventional annealing process, it typically takes a few minutes for the sample to reach thermal equilibrium with the furnace. In the rapid annealing process, where intense lamps are used to heat the sample, it only takes a few seconds to bring the sample to the required anneal temperature. We have used the system described below to study the electrical activation of Si implants in InGaAs.

The HEATPULSE 210T system is commercially available from A.G. Associates, and a dedicated microprocessor. The annealing chamber contains upper and lower banks of high-intensity, tungsten-halogen lamps and water-cooled, reflective walls. A quartz diffuser tube positioned between the lamp banks is hermetically sealed to the door with an O-ring. A flat piece of quartz with small pins attached to the door plate holds the wafer and loads it into the annealing chamber. The visible light emitted from the lamps passes through the quartz tube wall and the wafer tray and is absorbed by the wafer.

The banks contain thirteen 1.5 kW lamps. The maximum input power to the lamps is limited at 18 kW. This power is converted

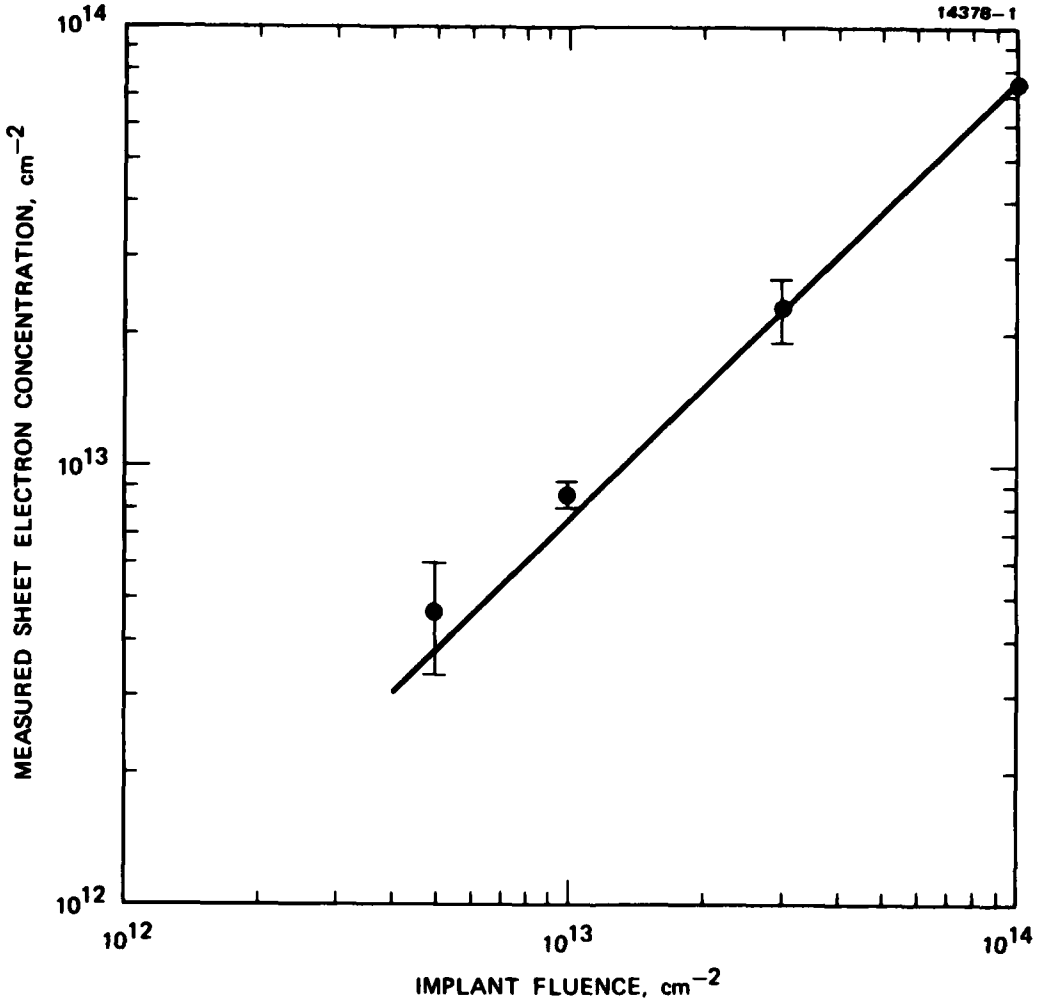

Figure 7. Measured sheet electron concentration as a function of implant fluence in Si-implanted InGaAs epitaxial layers annealed at 700°C for 30 minutes.

into radiant energy which is efficiently absorbed by the sample to be annealed. A schematic cross-section of the HEATPULSE system and a block diagram are shown in Figure 8.

A small Si-monitoring piece with a theromocouple glued to it is located in the annealing chamber. The thermocouple signal is fed to the controller, enabling closed-loop temperature monitoring and control. However, this type of monitoring has its own problems. The actual sample temperature for InGaAs may be different from the measured temperature.

In Figure 9 we show a trace of the monitor thermocouple output during an anneal sequence. The anneal temperature is ~700°C. The anneal time is defined as the time during which the sample is maintained at the anneal temperature. The microprocessor allows the rise time (t_r) and the fall time (t_f) to be independently controlled.

The results of the rapid thermal annealing experiments are summarized in Table 2. For comparison, we include the data from samples which were conventionally furnace annealed for 30 min. As seen from the data, a high degree of carrier activation can be achieved in as short an anneal time as 10 sec, at 750°C. The mobility recovery is much more gradual.

These studies clearly show that silicon is a well-behaved donor in $In_{0.53}Ga_{0.47}As$ and that high electrical activation can be achieved by annealing at temperatures between 700°C and 750°C. We have also demonstrated that high quality layers can be formed by rapid annealing procedures. In contrast, activation of p-type dopants (at least Be and Mg) appears to be a major problem in $In_{0.53}Ga_{0.47}As$.

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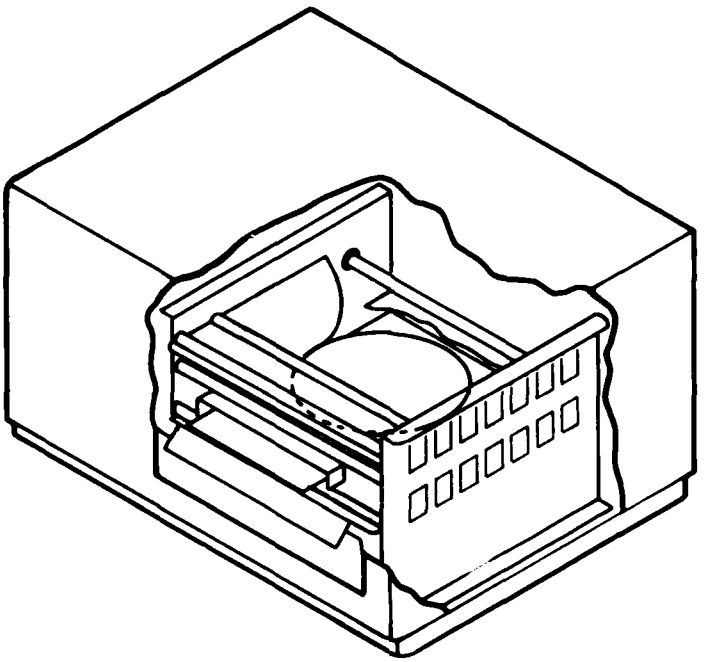
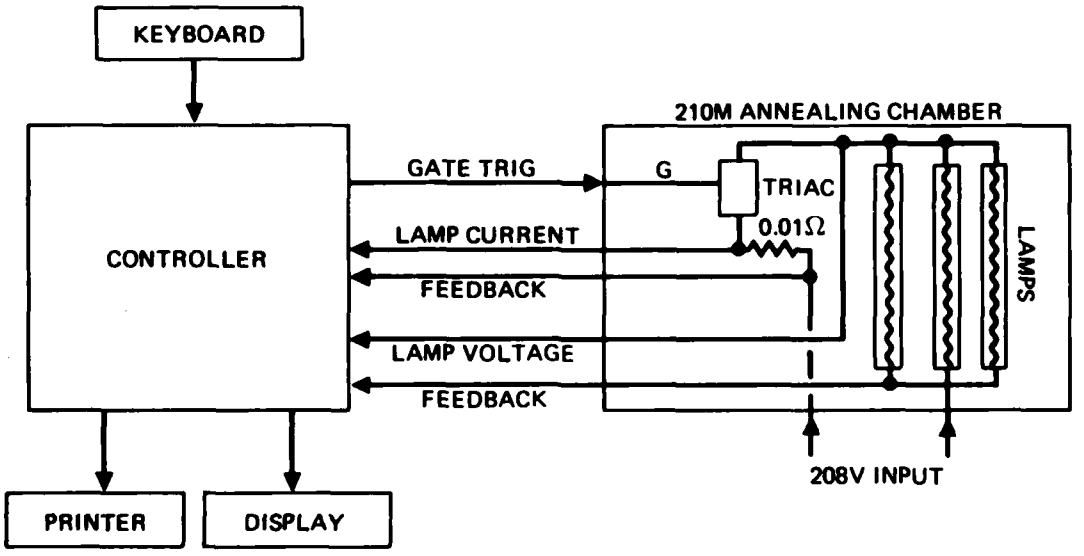


(a) CROSS SECTION



(b) BLOCK DIAGRAM

Figure 8. Schematic diagram of HEATPULSE 210M system.

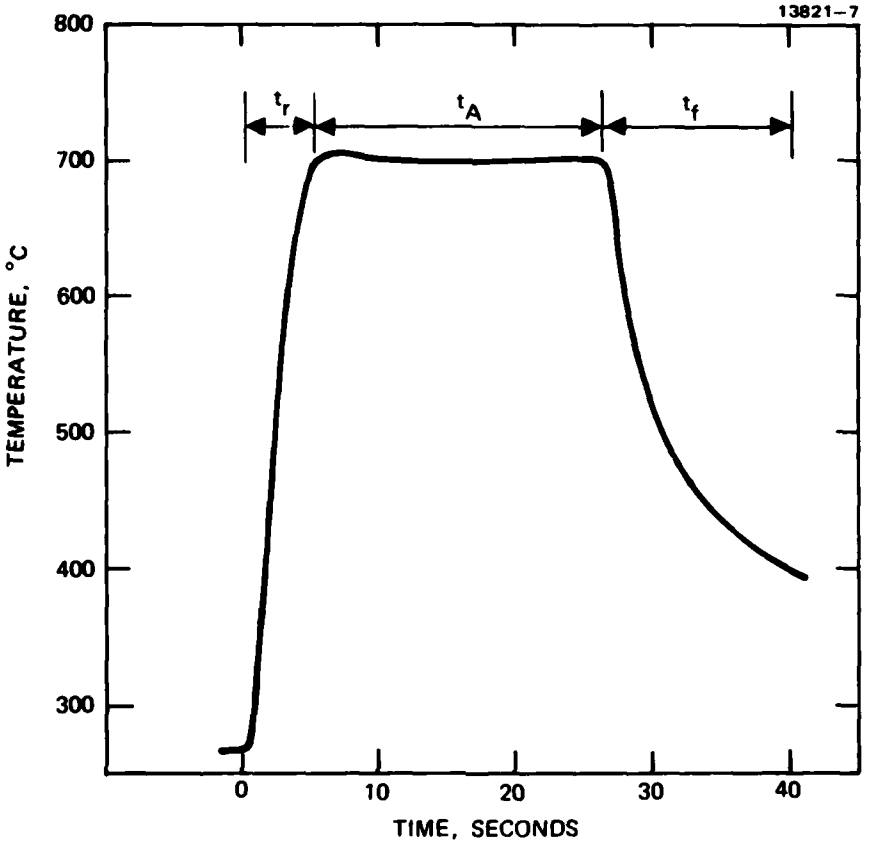


Figure 9. Typical time, temperature curve obtained from a measuring thermocouple in the heat pulse system.

Table 2. Electrical Properties of Rapid Thermally-Annealed and Furnace-Annealed (750°C) Si-Implanted $In_{0.53}Ga_{0.47}As$

DDSE	RTA 20 sec		RTAC 40 sec		Furnace, 30 min.	
cm^{-2}	Carrier Concentration (cm^{-2})	Mobility $cm^2V^{-1}s^{-1}$	Carrier Concentration (cm^{-2})	Mobility $cm^{-2}V^{-2}s^{-1}$	Carrier Concentration (cm^{-2})	Mobility $cm^2V^{-1}s^{-1}$
10^{13}	8.97×10^{12}	4140	8.7×10^{12}	4240	9×10^{12}	4940
10^{12}	8.5×10^{13}	3360	8.4×10^{13}	3620	8.2×10^{13}	4305

SECTION 4

CHARACTERIZATION OF InGaAs SURFACES

Development of mature InGaAs MISFET device technology is critically dependent on our understanding of the semiconductor-to-dielectric interface. As is the case for most other III-V semiconductor systems, InGaAs MISFETs have been fabricated using deposited dielectrics. The interface in such a case consists of the deposited dielectric as well as any native oxide present on the semiconductor surface. In this section we describe the results of experiments performed to elucidate the nature of the native oxide present on InGaAs surfaces, changes in the native oxide during subsequent dielectric deposition, and capacitance voltage measurements on InGaAs-native oxide-plasma deposited SiO_2 interface.

A. DESCRIPTION OF EXPERIMENTAL TECHNIQUES

Two spectroscopic techniques were used to study the chemical nature of the InGaAs surface: x-ray photoelectron spectroscopy (XPS) and electron energy loss spectroscopy (ELS). The experiments were performed using a VG Scientific ESCALAB Mark II spectrometer. The SiO_2 deposition was carried out using a Hughes-designed plasma deposition system.

B. X-RAY PHOTOEMISSION SPECTROSCOPY (XPS)

In this process an incident x-ray beam ionizes core electrons. Some of the ionized photoelectrons escape from the sample into vacuum and can be detected and energy analyzed. Knowing the incident photoenergy ($h\nu$) and the kinetic energy (K.E.) of the electrons emitted, one can calculate the binding energy of the electrons, BE, which is given by

$$BE = h\nu - K.E. \quad , \qquad (1)$$

where K.E. is the kinetic energy of the emitted electron. In our experiments, x-rays from a Mg target (Kα) with an energy of 1253 eV were used. In a typical XPS spectrum the number of electrons N(E) is displayed as a function of the binding energy. Thus, a peak in XPS spectrum is characterized by a certain energy and represents the electrons emitted from a certain atomic orbital.

Changes in the local chemical bonding (for example, indium bonded to oxygen versus In metal) may result in a chemical shift of the XPS peak. The observed chemical shifts can then be related to the nature of chemical bonding present in the analyzing volume. Electrostatic charging of the sample can create problems in determining the exact chemical shift. In the present work we have circumvented this potential problem by referencing all binding energies with respect to the omnipresent carbon peak at 284.6 eV. A major advantage of XPS stems from the fact that the photoelectron escape depth is less than ~100 Å and therefore can be used to non-destructively analyze native oxide/semiconductor and deposited oxide/semiconductor interfaces. In Figure 10 we schematically show the experimental arrangements as well as a stylized XPS spectrum.

C. ELECTRON ENERGY LOSS SPECTROSCOPY (ELS)

In this technique, a beam of low energy electons, typically < 1 keV, impinges on the sample surface. These primary electrons can undergo either elastic or inelastic scattering. Electrons scattered elastically change direction but do not suffer energy loss. This process is used in low energy electron diffraction (LEED). The inelastically scattered electrons suffer energy loss. This loss may either be due to excitation of surface or bulk plasmons or interband transitions. Again, some of the primary electrons escape from the sample and can be energy analyzed.

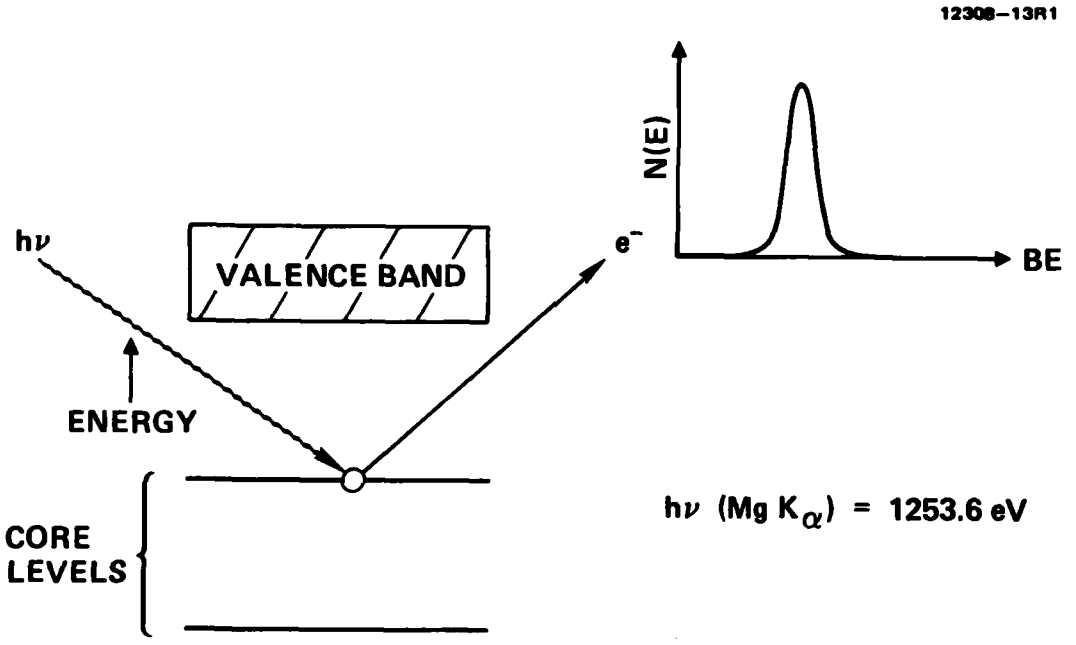


Figure 10. A schematic illustrating the XPS technique.

ELS measurements can be performed in two modes. In the first mode, the second derivative of the number of electrons with respect to energy ($- d^2N(E)/dE^2$) is plotted as a function of the energy loss, E_L. This technique is used when studying plasmons and valence-to-conduction band interband transitions. In the second mode, a very low energy primary beam (~10 eV) is used. A high resolution ELS spectrometer is required for these studies. Resolution of the elastic peak of FWLIM of ~10 meV is required in such measurements. This analysis is typically used study lattice vibrations.

The experiments described in this section were performed in the following manner. A standard Auger electron gun was used with a primary electron energy of 300 eV and a beam current of 10 nA. Data were collected directly in the N(E) mode using standard retarding potential and pulse-counting electronics. The resolution of the system was 0.55 eV FWHM. Very low beam currents can be used in this process, thereby avoiding the problem of electron beam damage to the analyzing surface. Because the spectrum is collected in the N(E) mode which is similar to surface sensitive optical absorption measurements, any absorption edges in the spectrum can be used to estimate bandgaps of surface compounds present and also to provide useful information regarding the trap structure of surface compounds. Finally, the collected N(E) spectrum can be double differentiated using a computer if needed. A schematic of the ELS process is presented in Figure 11.

D. EXPERIMENTAL RESULTS

1. Analysis of Native Oxide

InGaAs epitaxial layers grown by LPE and lattice matched to InP substrates were first subjected to a thorough cleaning process. The n-type layers were nominally undoped, with a carrier concentration of ~5 x 10^{-15} cm^{-3}. These layers were then

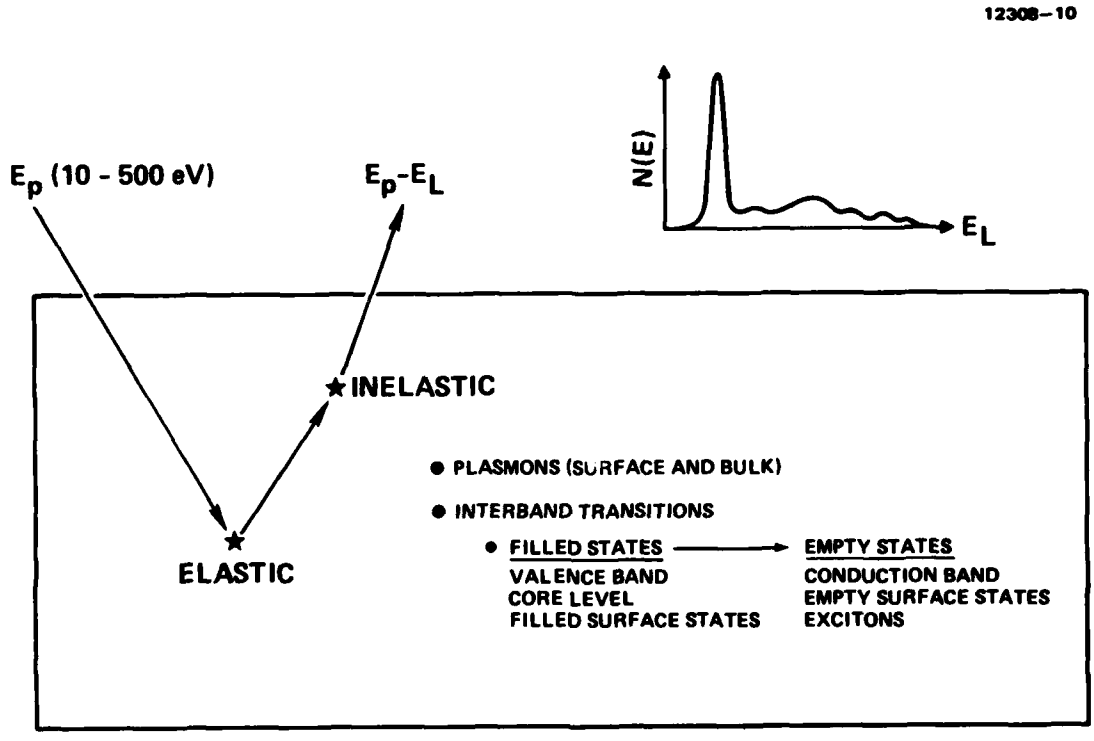


Figure 11. A schematic illustrating the ELS technique.

etched for ~1 min in a solution of 1:2:400 parts by volume of $NH_4OH:H_2O_2:H_2O$, for 30 sec in a solution of 1:15 parts by volum e of $NH_4OH:H_2O$, and rinsed in a 4:1 mixture of methanol and acetone and blown dry in nitrogen. After etching, the samples were exposed to ambient air for ~1 hour before loading into the VG ESCALAB Mark II system for analysis.

XPS studies were performed on these etched surfaces using the procedures described earlier. Carbon and oxygen were the only detectable contaminants on the surface.

In Figure 12 we illustrate the XPS spectrum of the As 3-d states. The spectrum consists of two well-defined peaks. The As substrate peak is located at a binding energy of 40.4 eV, while the second weaker peak is located at 43.9 eV, with an energy separation of 3.5 eV between the two peaks. The position and shape of the major As peak is consistent with bonded As. No metallic As is observed. The weaker peak is related to oxidized As; its binding energy is consistent with that of As_2O_3.

In Figure 13 we show the In $3d_{5/2}$ XPS spectrum. The spectrum again shows clear evidence of two peaks, at 444.2 eV and 445.0 eV. The 444.2 eV peak is related to the InGaAs substrate, while the 445.0 eV peak is related to the presence of oxidized indium. The observed binding energy of the oxidized In peak is too high for In_2O_3. Clark et al.[3] report a binding energy of 444.4 eV for In_2O_3, while Bertrand[4] claims it to be 444.3 eV. Our observed binding energy of 445.0 indicates that the dominant oxide in this case is not In_2O_3. Potential candidates include $InAsO_4$, InO-OH, $In(OH)_3$, etc. More work is required to resolve this issue.

The XPS spectrum obtained from Ga 3d/In4d levels is quite complex and is rather difficult to interpret. It clearly showed the presence of oxidized In; however, it was not clear from this spectrum whether gallium oxide was present or not. From heat-of-formation considerations, one would expect to find oxidized gallium.

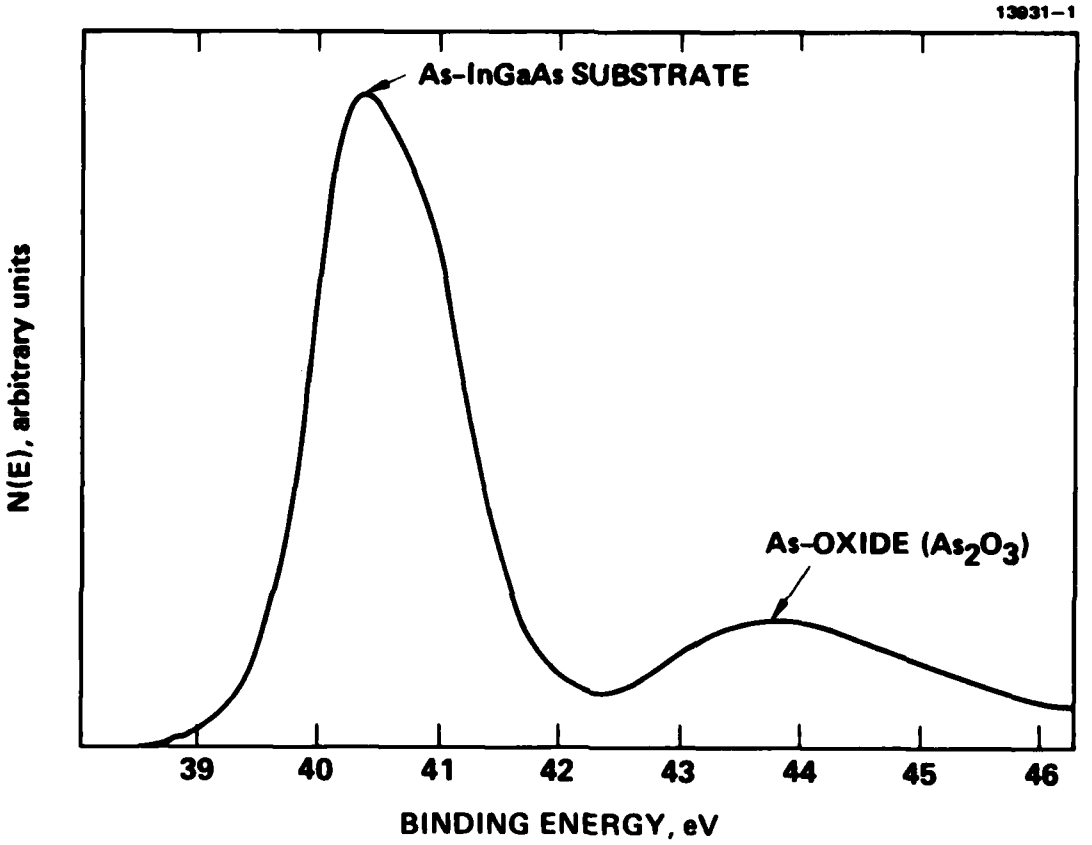


Figure 12. XPS As 3d spectrum from air-oxidized InGaAs.

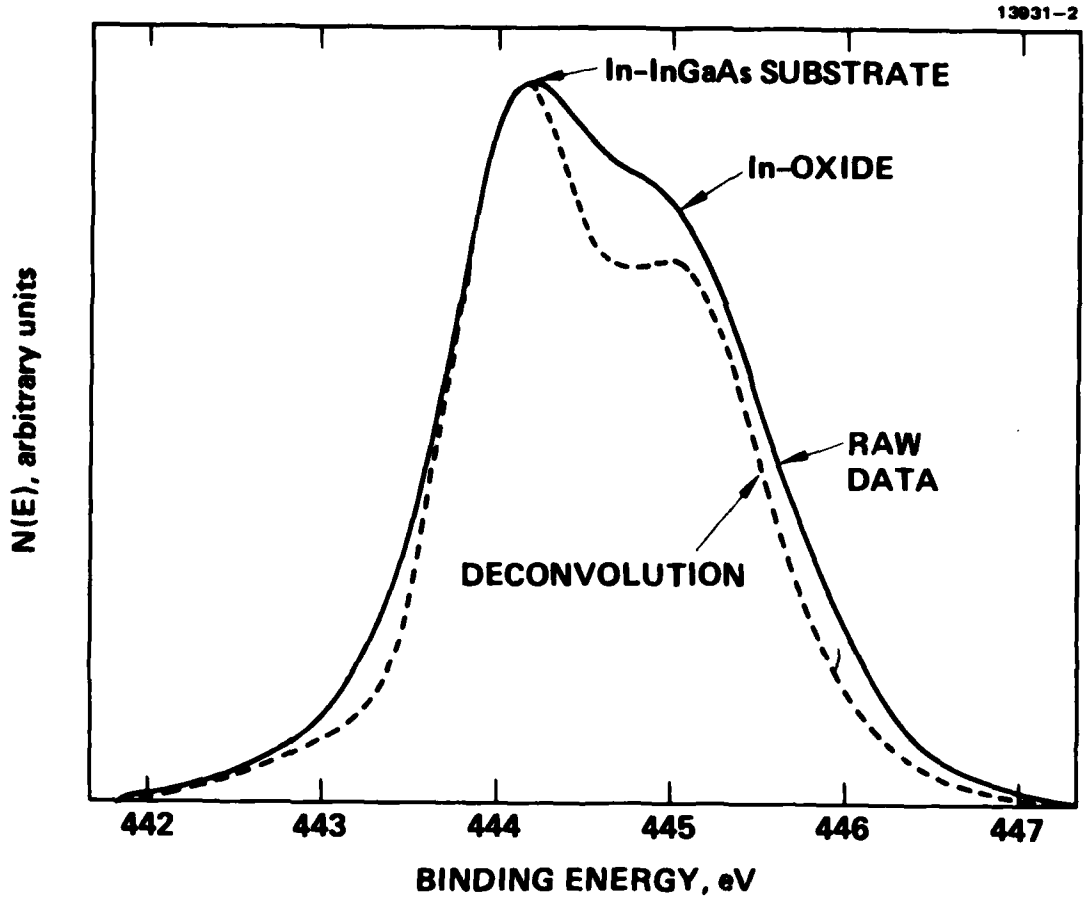


Figure 13. XPS in $3d_{5/2}$ spectrum from air-oxidized InGaAs. The deconvolution spectrum has been corrected for system broadening.

We therefore decided to perform detailed XPS measurement on Ga at the $2p_{3/2}$ level. Spectra were obtained with two different take-off angles, 0° and 50°, respectively. In Figure 14, we show the 0° spectrum. A substrate peak at 117.8 eV and an oxide peak at 1118.2 eV can be seen. The oxide peak is more clearly evident in the 50° take-off spectrum (which is more surface sensitive), as seen in Figure 15. Clearly, more detailed work is required before we can unambigiously determine the exact oxidation state of gallium.

We estimate the thickness of the native oxide to be ~6 A from the As 3d data, to be ~15 A from In data, and ~18 A from Ga data. We can also estimate the "near surface" composition of the $In_{0.53}Ga_{0.47}As$ layers (see Table 3). From these data, it is clear that while the measured In concentration is close to the bulk composition, the surface is gallium-rich and As-deficient. This near surface composition may be extremely sensitive to the nature of surface treatment that the InGaAs layer undergoes prior to analysis.

The electron energy loss spectroscopy (ELS) spectrum is illustrated in Figure 16. The primary electron energy used was 303.5 eV. The ELS spectrum shows an absorption edge at 2·1eV and an interband transition at 6.4 eV. We have measured the ELS spectra of etched GaAs and oxidized In surfaces. Comparison of these data suggests that the ELS spectrum on an etched InGaAs surface is dominated by the presence of In oxide, similar to In_2O_3. Again, more careful analysis is required in order to understand the condition of chemically etched $In_{0.53}Ga_{0.47}As$ surfaces.

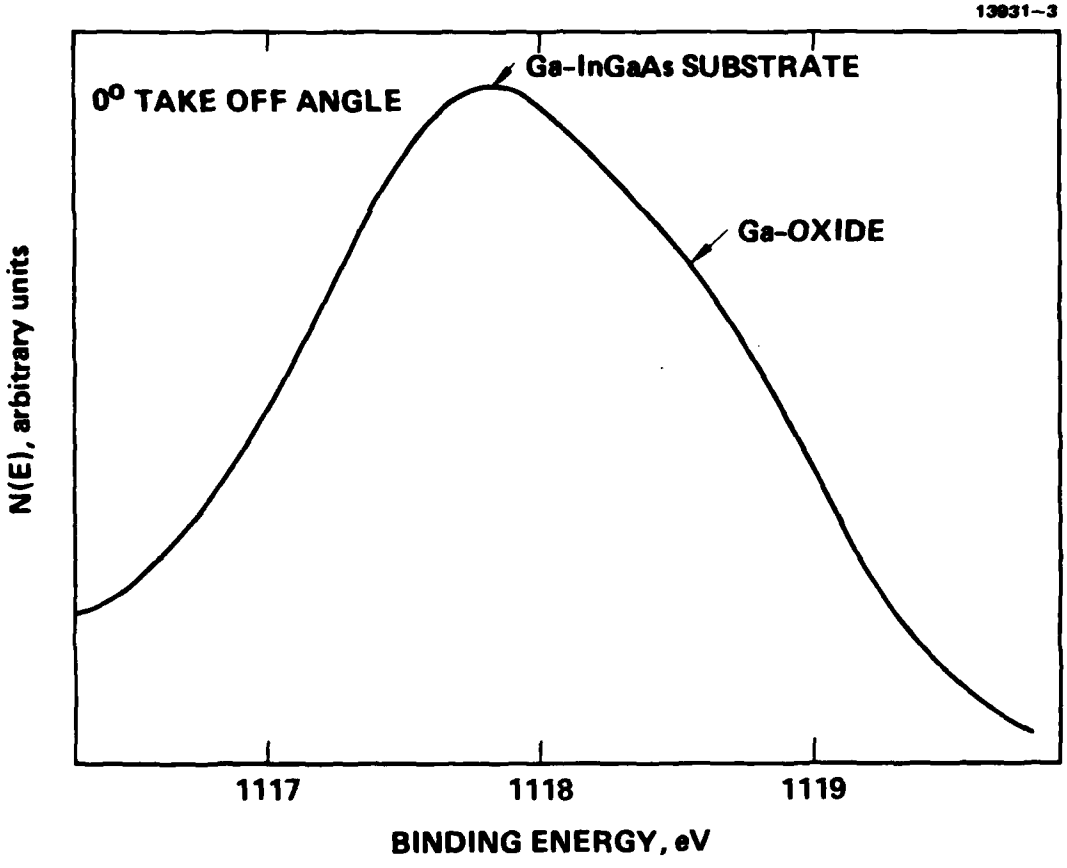


Figure 14. XPS Ga $2p_{3/2}$ spectrum from air-oxidized InGaAs taken at a take-off angle of 0°.

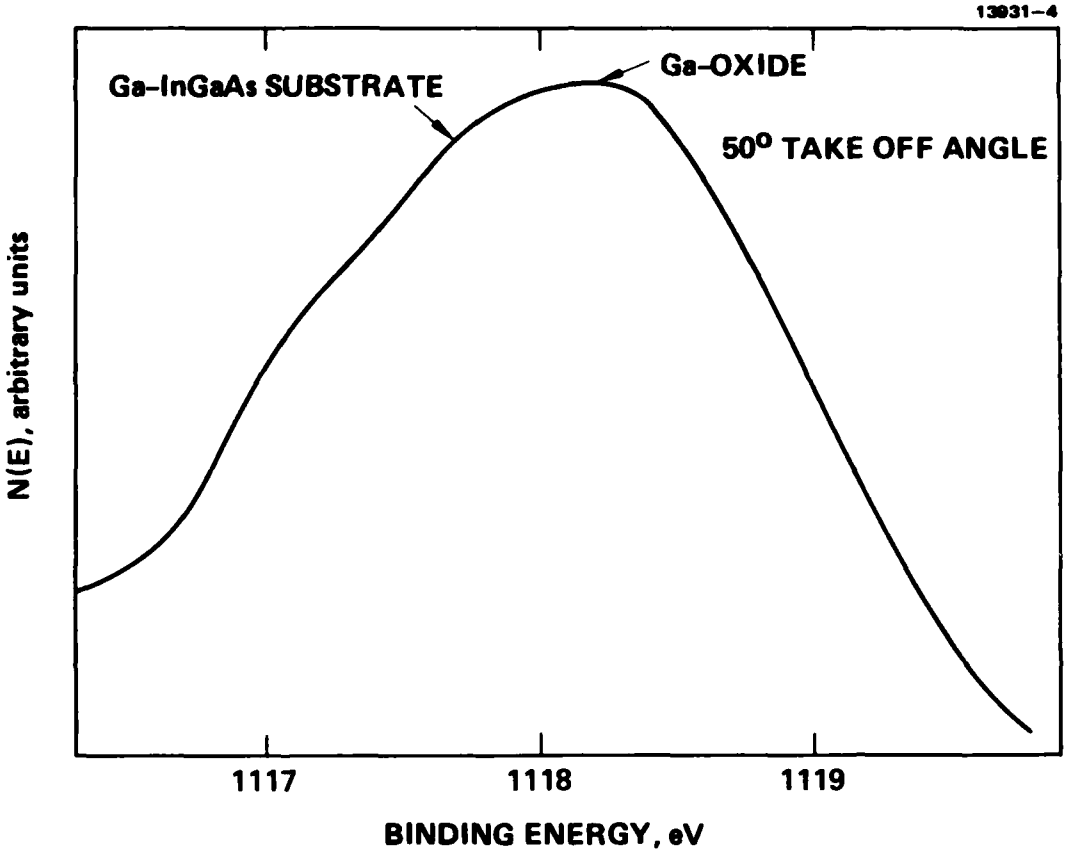


Figure 15. XPS Ga $2p_{3/2}$ spectrum from air-oxidized InGaAs taken at a take-off angle of 50°. This condition is more surface-sensitive.

Table 3. Measured Composition of the Near Surface Region of $In_{0.53}Ga_{0.47}As$ Layers as Compared with Theoretical Composition

Line	Measured Atomic %	Theo. Atomic %
In $3d_{5/2}$	25	26.5
In 4d	24	26.5
Ga 3d	34	23.5
As 3d	41	50

2. Analysis of Deposited SiO_2/Native Oxide Interface

a. XPS Studies

As long as the deposited SiO_2 layer is thin (~30-40 A), it is possible to analyze the entire semiconductor/native oxide/deposited SiO_2 structure non-destructively using x-ray photoemission spectroscopy (XPS). We prepared such structures shown schematically in Figure 17. The SiO_2 layer was deposited by a plasma-enhanced deposition process at 300°C in a system developed at Huqhes Research Laboratories. Detailed XPS measurements were performed on these structures. Within the resolution of the experimental techniques employed, we concluded that the plasma enhanced deposition process does not significantly increase or reduce the thickness of the native oxide present on the surface prior to dielectric deposition.

b. C-V Analysis

We performed C-V measurements on MIS capacitors fabricated on InGaAs epi-layers. Soldered In contacts provided the ohmic contact. Plasma enhanced SiO_2 deposited at 300°C was used as the dielectric, with Al as the gate metal. Quasi-static, 10 kHz and 1 MHz C-V measurements were made on these capacitors.

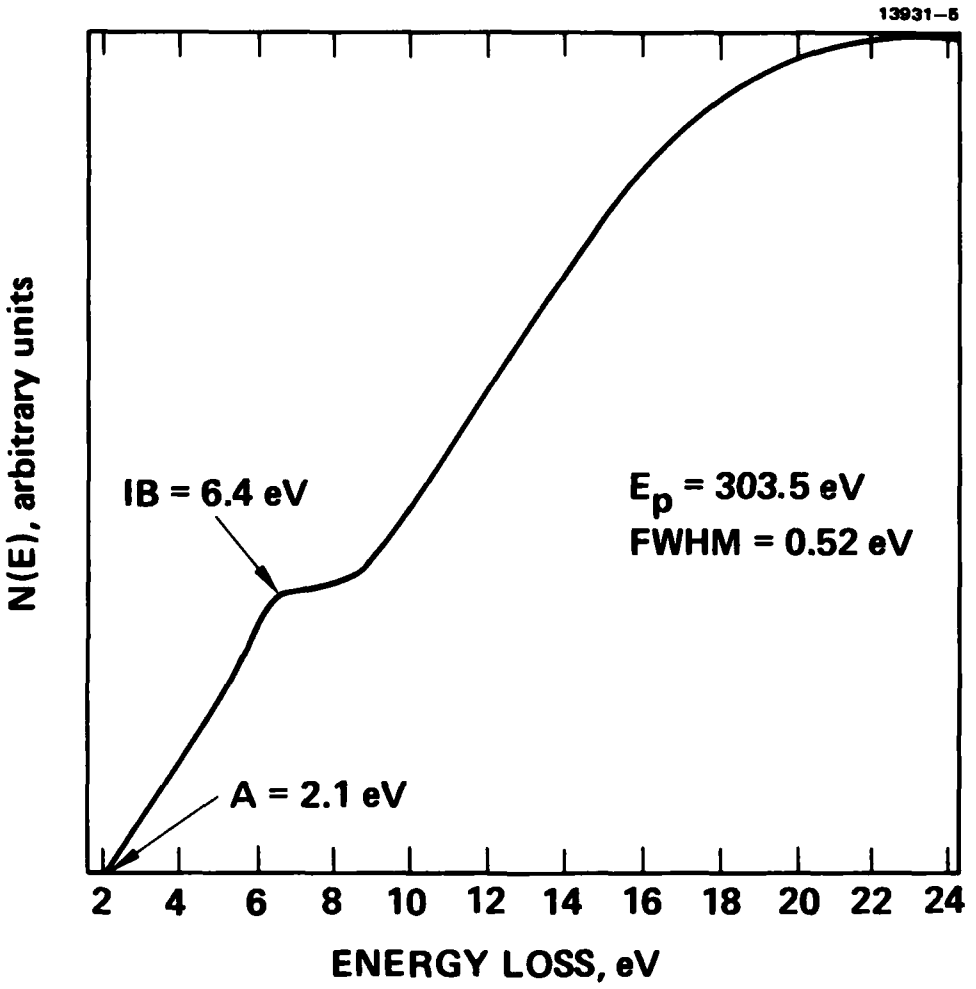


Figure 16. ELS spectrum from air-oxidized InGaAs.

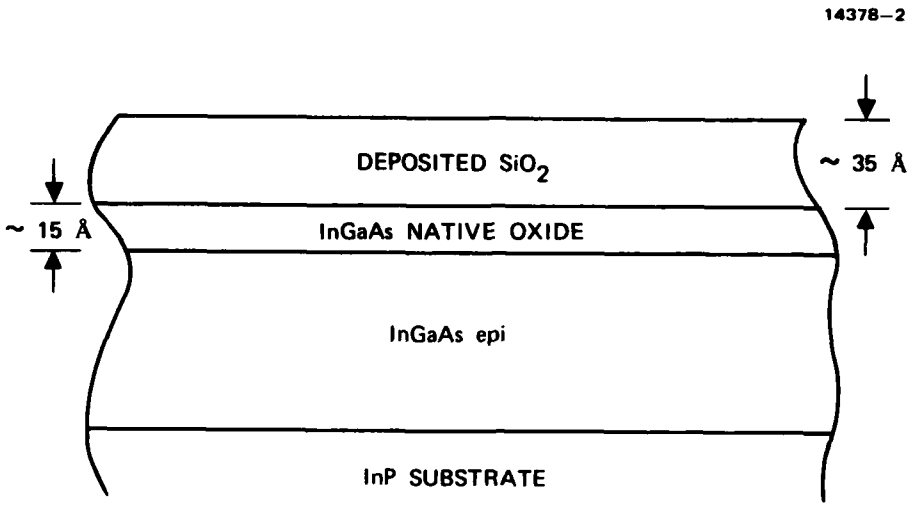


Figure 17. Schematic of the sample used for XPS studies in Section 4.D.2(a).

The ability to make quasi-static measurements clearly indicates that the dielectric is of high quality with resistivities higher than ~10^{15} Ω - cm. Typical 10 kHz and 1 MHz C-V data is shown in Figure 18. The clockwise hysteresis is clearly an indication of electron injection into the dielectric.

From an analysis of quasi-static and 1 MHz C-V cures, we concluded that the surface state densities are quite high. We have conservatively estimated the minimum value ~4.6 x 10^{12} cm^{-2} V^{-1}. These numbers are very similar to surface state densities reported by Tell et al. and Gourner et al.

On the basis of these preliminary surface studies, we conclude that the native oxides present on $In_{0.53}Ga_{0.47}As$ are thin. It is possible to modify the nature of native oxides by appropriate chemical treatment. The process of depositing SiO_2 by a plasma-enhanced process does not significantly affect the thickness of the native oxide. The quality of PECVD SiO_2 is adequate to fabricate MIS devices in $In_{0.53}Ga_{0.47}As$.

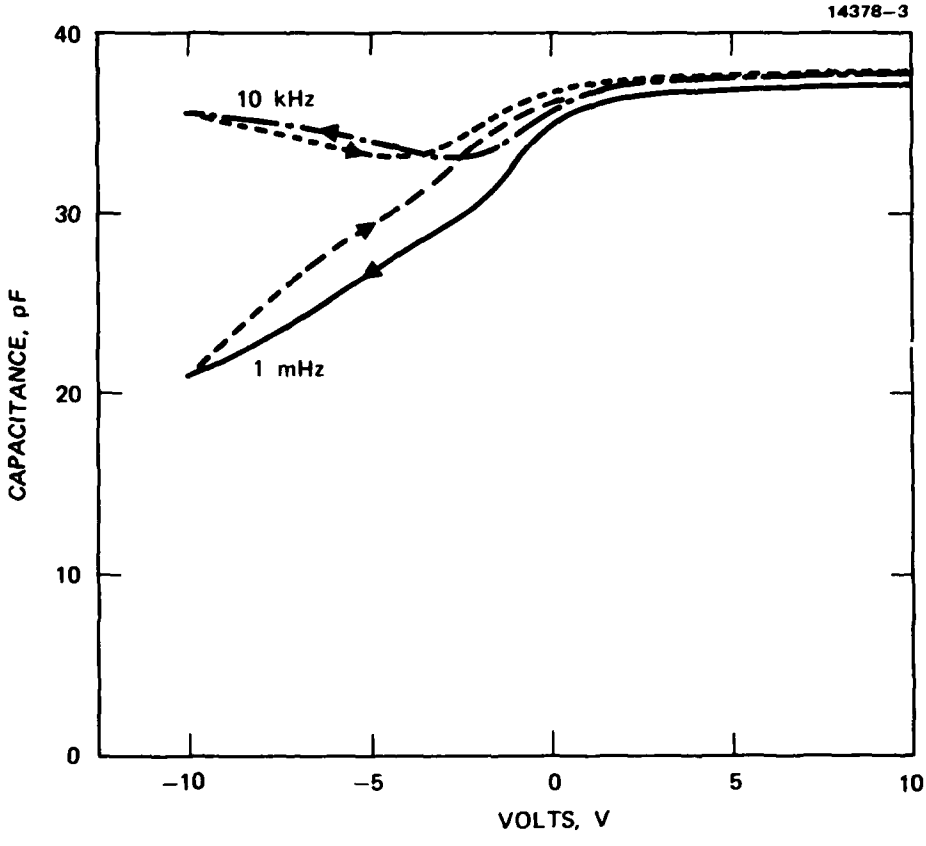


Figure 18. Typical capacitance-voltage characteristics of $Al/SiO_2/In_{0.53}Ga_{0.47}As$ capacitors. The sweeprate used was 100 MV/s.

SECTION 5

SUMMARY

In summary, our studies lead us to the following conclusions:

- Major unresolved technical problems remain in applying the infinite solution technique to the growth of $In_{0.53}Ga_{0.47}As$ epitaxial layers lattice-matched to InP matched to InP substrates. The inability to reduce stable In oxides present on InP substrates at the lower growth temperatures is a major problem area. This problem can be solved by growing at higher temperatures (> 600°C). However, at higher growth temperatures the growth rate is is too high.

- Silicon is a well-behaved donor dopant in $In_{0.53}Ga_{0.47}GaAs$. It can be introduced by ion implantation, and a high degree of donor activation in $In_{0.53}Ga_{0.47}As$ can be achieved by annealing at temperatures in the range 700°C to 750°C.

- A rapid thermal anneal procedures is effective in activating silicon donors with anneal times as low as 10 seconds.

- Activation of p-type dopants in $In_{0.53}Ga_{0.47}As$ introduced by ion implantation is extremely difficult.

- Thin native oxides (~ 15 Å) are present on etched surfaces of $In_{0.53}Ga_{0.47}As$. The oxidation state of As is As_2O_3. The oxidation states of In and Ga are not well defined. The near surface region of InGaAs surfaces is Ga-deficient.

- High quality SiO_2 layers can be deposited on $In_{0.53}Ga_{0.47}As$ by a plasma-enhanced process. The dielectric deposition process does not perturb the native oxide present prior to deposition. Even though the surface state densities are quite high, it appears that SiO_2 can be used as a gate dielectric for $In_{0.53}Ga_{0.47}As$ MISFETs.

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